**DETAILED ACTION**

**EXAMINER'S AMENDMENT**

1. An examiner's amendment to the record appears below. Should the changes and/or additions be unacceptable to applicant, an amendment may be filed as provided by 37 CFR 1.312. To ensure consideration of such an amendment, it MUST be submitted no later than the payment of the issue fee.

2. Authorization for this examiner's amendment was given in a telephone interview with Attorney Joseph B. Ryan on the 24th September 2008. Discussed providing further clarifications to the claims with regards to M entries and N counters, and detail that the counter is reset only a single time within the time window.

3. The application has been amended as follows:

1. (Currently amended) A processor comprising:

controller circuitry operative to control performance of a continuity check for each of a plurality of flows of protocol data units received by the processor; and

memory circuitry comprising a continuity check cache;

wherein the continuity check cache stores an identifier for each of a subset of the plurality of flows;

wherein the controller circuitry controls access to a set of continuity check counters comprising a counter for each of the plurality of flows;

the controller circuitry determining if a given flow for which a protocol data unit is received in the processor has a corresponding entry in the continuity check cache, and if the given flow has such an entry, preventing a corresponding one of the continuity check counters from being updated, and if the given flow does not have such an entry, clearing the corresponding one of the continuity check counters and storing a flow identifier for the given flow in the continuity check cache;

wherein the continuity check cache has a capacity of M entries, a given one of which may correspond to the flow identifier, and the set of continuity check counters includes N continuity check counters, where M is substantially less than N.

2. (Original) The processor of claim 1 wherein the memory circuitry comprises an internal memory of the processor, and the continuity check cache is implemented in its entirety within the internal memory.

3. (Original) The processor of claim 1 wherein the set of continuity check counters are stored in an external memory associated with the processor.

4. (Original) The processor of claim 1 wherein at least one of the continuity checks is performed in a manner compliant with an I.610 protocol.

5. (Original) The processor of claim 1 wherein at least one of the protocol data units comprises a cell.

6. (Canceled)

7. (Original) The processor of claim 1 wherein one or more of the flows correspond to particular network connections.

8. (Original) The processor of claim 1 wherein each of the flows for which a flow identifier is stored in the continuity check cache has had its corresponding continuity check counter cleared upon receipt of a first protocol data unit for that flow within a specified time window.

9. (Original) The processor of claim 1 wherein each of the continuity check counters is configured so as to be incremented if one or more protocol data units are not received for the corresponding flow within a specified time window.

10. (Previously presented) The processor of claim 1 wherein in conjunction with the continuity check performed for the given flow the continuity check fails and a timeout indication is generated if the corresponding continuity check counter reaches a particular value.

11. (Currently amended) ~~The processor of claim 1~~ A processor comprising:

controller circuitry operative to control performance of a continuity check for each of a plurality of flows of protocol data units received by the processor; and

memory circuitry comprising a continuity check cache;

wherein the continuity check cache stores an identifier for each of a subset of the plurality of flows;

wherein the controller circuitry controls access to a set of continuity check counters comprising a counter for each of the plurality of flows;

the controller circuitry determining if a given flow for which a protocol data unit is received in the processor has a corresponding entry in the continuity check cache, and if the given flow has such an entry, preventing a corresponding one of the continuity check counters from being updated, and if the given flow does not have such an entry, clearing the corresponding one of the continuity check counters and storing a flow identifier for the given flow in the continuity check cache;

wherein in conjunction with the continuity check performed for the given flow a corresponding one of the continuity check counters is reset only a single time for a plurality of protocol data units received by the processor for the given flow within a specified time window.

12. (Original) The processor of claim 1 wherein at least one of the continuity check counters comprises a multi-bit counter with each increment of the count representing a specified time window within a designated period of time for which the continuity check is performed.

13. (Original) The processor of claim 1 wherein at least one of the continuity check counters comprises a three-bit counter with each increment of the count corresponding to a time window having a duration of approximately 0.5 seconds.

14. (Original) The processor of claim 1 wherein the entries of the continuity check cache are cleared after expiration of each of a plurality of time windows for which the continuity check counters can be incremented.

15. (Previously presented) The processor of claim 1 wherein if the continuity check cache is full when one of the plurality of flows first arrives at the processor, a particular flow identifier from the cache is removed to make room for storage of the flow identifier for the arriving flow.

16. (Original) The processor of claim 1 wherein the processor is configured to provide an interface for communication of the received protocol data units between a network and a switch fabric.

17. (Original) The processor of claim 1 wherein the processor comprises a network processor.

18. (Original) The processor of claim 1 wherein the processor is configured as an integrated circuit.

19. (Currently amended) A method for use in a processor comprising controller circuitry operative to control performance of a continuity check for each of a plurality of flows of protocol data units received by the processor, the controller circuitry being further operative to control access to a set of continuity check counters comprising a counter for each of the plurality of flows, the method comprising the steps of:

storing an identifier for each of a subset of the plurality of flows in a continuity check cache; and

determining if a given flow for which a protocol data unit is received in the processor has a corresponding entry in the continuity check cache, and if the given flow has such an entry, preventing a corresponding one of the continuity check counters from being updated, and if the given flow does not have such an entry, clearing the corresponding one of the continuity check counters and storing a flow identifier for the given flow in the continuity check cache;

wherein the continuity check cache has a capacity of M entries, a given one of which may correspond to the flow identifier, and the set of continuity check counters includes N continuity check counters, where M is substantially less than N.

20. (Currently amended) An article of manufacture comprising a computer readable medium having at least one computer program encoded therein for use in a processor comprising controller circuitry operative to control performance of a continuity check for each of a plurality of flows of protocol data units received by the processor, the controller circuitry being further operative to control access to a set of continuity check counters comprising a counter for each of the plurality of flows, the at least one program when executed in the processor implementing the steps of:

storing an identifier for each of a subset of the plurality of flows in a continuity check cache; and

determining if a given flow for which a protocol data unit is received in the processor has a corresponding entry in the continuity check cache, and if the given flow has such an entry, preventing a corresponding one of the continuity check counters from being updated, and if the given flow does not have such an entry, clearing the corresponding one of the continuity check counters and storing a flow identifier for the given flow in the continuity check cache;

wherein the continuity check cache has a capacity of M entries, a given one of which may correspond to the flow identifier, and the set of continuity check counters includes N continuity check counters, where M is substantially less than N.

***Allowable Subject Matter***

4. The following is an examiner's statement of reasons for allowance:

The prior art fails to disclose the determination made as to whether the given flow (an identifier of the given flow) matches an entry in the continuity check cache, and a determination is made as to whether or not a match exists between the identifier of the given flow and any particular cache entry. If there is not a hit for the given flow in the cache, this indicates that the corresponding continuity check counter in external memory has not yet been reset in the current time window (0.5 secs). Therefore, in the corresponding continuity check counter in external memory is cleared (reset to zero) and an identifier of the given flow is stored in the continuity check cache. The process then returns to process the next user cell received on the given flow or any other flow in the same time window. If there is a hit for the given flow in the cache, this indicates that the corresponding continuity check counter in external memory was already reset once in the current time window. Therefore, the corresponding continuity check counter is not accessed or otherwise updated based on the user cell received. This saves unnecessary external memory access. The closest prior art made of record are Park et al. (US 5872770) and Jourdan et al. (US 6505293 B1).

Any comments considered necessary by applicant must be submitted no later than the payment of the issue fee and, to avoid processing delays, should preferably

accompany the issue fee. Such submissions should be clearly labeled "Comments on Statement of Reasons for Allowance."

Any inquiry concerning this communication or earlier communications from the examiner should be directed to ABDULLAH RIYAMI whose telephone number is (571)270-3119. The examiner can normally be reached on Monday through Thursday 8am-5pm EST.

If attempts to reach the examiner by telephone are unsuccessful, the examiner's supervisor, Huy D. Vu can be reached on (571) 272-3155. The fax phone number for the organization where this application or proceeding is assigned is 571-273-8300.

Information regarding the status of an application may be obtained from the Patent Application Information Retrieval (PAIR) system. Status information for published applications may be obtained from either Private PAIR or Public PAIR. Status information for unpublished applications is available through Private PAIR only. For more information about the PAIR system, see http://pair-direct.uspto.gov. Should you have questions on access to the Private PAIR system, contact the Electronic Business Center (EBC) at 866-217-9197 (toll-free). If you would like assistance from a USPTO Customer Service Representative or access to the automated information system, call 800-786-9199 (IN USA OR CANADA) or 571-272-1000.

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